WHAT IS CLAIMED IS:

1. A data processing node within a multi-node multiprocessor system, comprising:

a processor connected to a system memory having a predetermined range of memory addresses;

a cache memory connected to the processor; and

a cache directory containing coherency status information for the range of memory addresses, wherein the cache directory is enabled to receive a message from a home node of a function, the message being indicative of the function and a list of operands and wherein a memory address for at least one of the operands is in the range of memory addresses; and

wherein the cache directory is enabled to determine a target node based, at least in part, on the cache coherency status information and memory access latency evaluation and to ship the function to the determined target node for execution.

2. The node of claim 1, wherein the cache directory determines the target node by determining whether there is a predominant node based on the list of operands, wherein a cache memory of the predominant node contains valid copies of more of the operands than the cache memory of any other node in the system.

3. The node of claim 1, wherein the cache directory determines the target node by prioritizing a set of candidate nodes according to loading information indicative of the loading on each of the nodes.

4. The node of claim 1, wherein the cache directory determines the target node by prioritizing a set of candidate nodes, at least in part, based on proximity information indicative of the architectural proximity of the candidate node.

5. The node of claim 1, wherein the cache directory is further enabled to retrieve cache coherency information from a remote directory for at least one of the list of operands and to use the retrieved cache coherency information in determining the target node.

6. The node of claim 5, wherein the cache directory is further enabled to update the node's cache memory responsive to determining an operand in the list of operands that is not valid in the cache memory.

7. A multiprocessor system, comprising:

a plurality of data processing nodes, each node having a processor coupled to a system memory, a cache memory, and a cache directory wherein the cache directory contains cache coherency information for a predetermined range of system memory addresses and wherein each node is enabled to initiate a function shipping request;

an interconnection enabling the nodes to exchange messages;

wherein each node initiating a function shipping request is enabled to identify a destination directory based on the list of operands associated with the function and to send a node determination message indicating a function and a list of corresponding operands to the identified destination directory; and

wherein each cache directory is enabled to determine a target node based, at least in part, on its cache coherency status information and memory access latency evaluation responsive to receiving the node determination message and to ship the function to the target node over the interconnection.

8. The system of claim 7, wherein a node initiating the request determines the destination directory by determining the directory that is the home directory to the greatest number of the list of operands.

9. The system of claim 7, wherein the destination directory determines the target node by determining whether there is a predominant node based on the list of operands, wherein the predominant node has a cache memory and further wherein the predominant node cache memory contains valid copies of more of the operands than the cache memory of any other node in the system.

10. The system of claim 9, wherein the destination directory determines the target node by prioritizing a set of candidate nodes when there is no predominant node, wherein the candidate nodes are prioritized according to loading information indicative of the loading on each of the nodes.

11. The system of claim 9, wherein the cache directory determines the target node by prioritizing a set of candidate nodes when there is no predominant node, wherein the candidate nodes are prioritized, at least in part, based on proximity information indicative of the architectural proximity of the candidate node.

12. The system of claim 7, wherein the destination directory is further enabled to retrieve cache coherency information from a remote directory for at least one of the list of operands and to use the retrieved cache coherency information in determining the target node.

13. The system of claim 12, wherein the destination directory is further enabled to update the node's cache memory responsive to determining an operand in the list of operands that is not valid in the cache memory.

14. A data processing system within a multi-node data processing network, comprising:

a microprocessor coupled to a system memory having a predetermined range of memory addresses;

a cache memory accessible to the processor;

a cache directory containing current cache coherency information for the range of memory addresses and further including means for receiving a list of memory addresses and for determining a target node from the list based, at least in part, on the cache coherency information and memory access latency evaluation.

15. The system of claim 14, wherein determining a target node includes determining the data locality of at least some of the operands wherein the data locality indicates on which cache directories within the multi-node system an operand is valid.

16. The system of claim 15, wherein determining a target node includes selecting a predominant node as the target node, wherein the predominant node contains valid copies of more function operands than any other node in the system.

17. The system of claim 14, wherein the system is further enabled to initiate a function shipping request and to identify an intermediate node on which to determine the target node for the request based on the home nodes of the request operands.

18. The system of claim 17, wherein the system identifies the intermediate node by identifying the node that is home node to the greatest number of operands.

19. The system of claim 18, wherein the system is further enabled to import cache coherency data for operands having home nodes that differ from the intermediate node, and to use the imported cache coherency data in determining the target node.

20. The system of claim 14, wherein determining the target node further includes determining the target node based on information including loading information and architectural proximity information.